Lecture: Deep Learning and Differential Programming

3.3 GPUs - Software

https://liris.cnrs.fr/christian.wolf/teaching



APIs

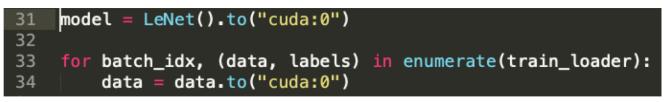
GPUs can be programmed on multiple different levels of abstraction.

We will (very briefly) study two cases:

CUDA/C++: direct low-level GPU programming

1 __global__ 2 void mult_kernel_simple(int mxWidth, float *mx1, float *mx2, float *output) 3 { 4 int c = blockIdx.x*blockDim.x + threadIdx.x;

PyTorch/Python: high-level of abstraction

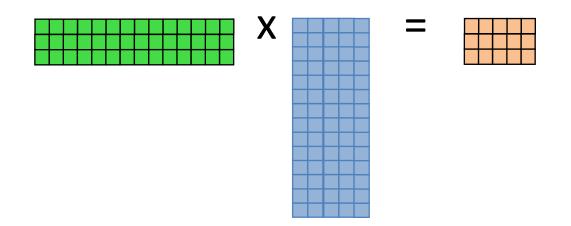


1 CUDA – low level GPU programmng

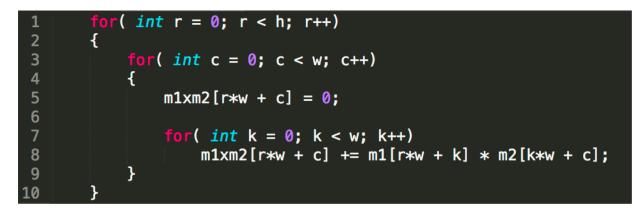
2 GPUs & PyTorch



Example : matrix multiplication

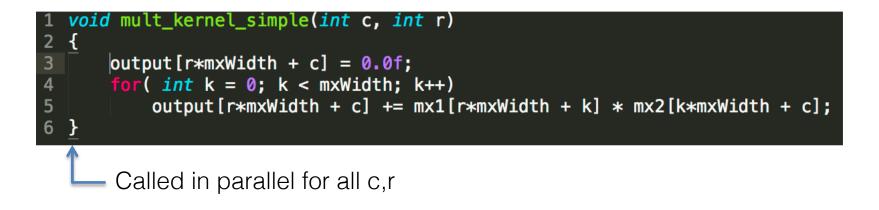


The classical sequential solution:



The parallel solution

Parallel execution of a function called for each individual result value of the result matrix, with arguments being the indices of the value.

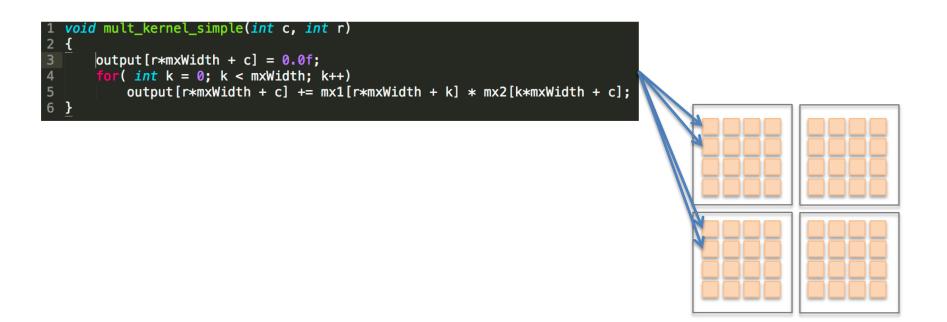


In CUDA, this function is called a *kernel*. Each tuple (c,r) corresponds to a *thread*.



Organisation into blocks

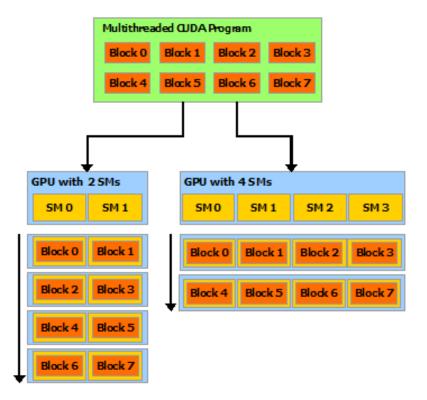
- Threads are organized into *blocks*
- Faster local memory can be shared by threads of the same block.





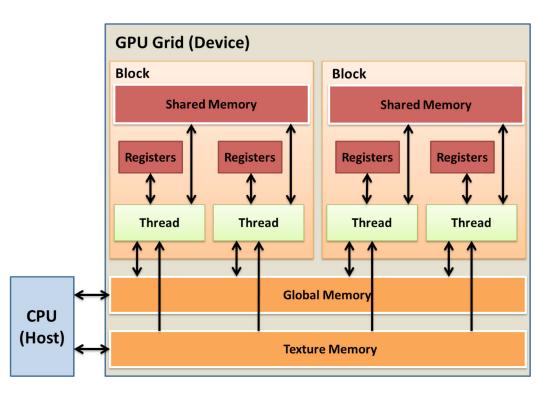
SM

A block will be sent to a SM (*streaming multi-processor*)



The classical CUDA sequence

- The CPU allocates memory on the GPU
- The CPU copies the data to GPU global memory
- The CPU launches the kernel on the GPU
- The GPU executes the kernel in parallel
- The CPU copies the result data back to CPU host memory



The CUDA syntax of the kernel

Key word declares the kernel



Index of the block in the grid

Index of the thread in the block

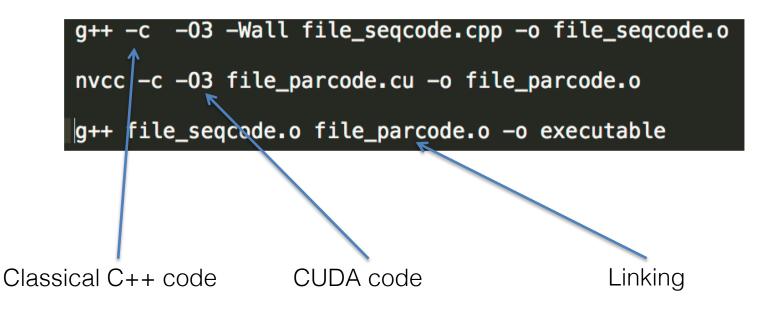
Calling the kernel

```
int main(void)
   {
 2
 3
        . . .
       // allocate memory on GPU
 4
 5
       cudaMalloc( (void**) & gpuMatrix1, matrixSizeInBytes);
 6
        . . .
 8
       // copy data from CPU memory to GPU memory
 9
       cudaMemcpy(gpuMatrix1, matrix1, matrixSizeInBytes, cudaMemcpyHostToDevice);
10
        . . .
11
12
       // Set grid and block size
13
       dim3 dimBlock(32, 32);
14
       dim3 dimGrid(matrixWidth/dimBlock.x, matrixWidth/dimBlock.y);
15
16
       // run kernel
17
       mult_kernel_simple<<<dimGrid, dimBlock>>>( matrixWidth, gpuMatrix1, gpuMatrix2, gpu0
18
       // copy back results from GPU memory to CPU memory
19
20
        cudaMemcpy( outputData, gpuOutput, matrixSizeInBytes, cudaMemcpyDeviceToHost);
21
        . . .
22
```

Call the *kernel* in parallel for a set of threads

Compilation

CUDA uses a specific compiler, which is based on a generic C++ compiler (gcc)



Debugging and profiling

The nvvp profiler is part of the CUDA toolkit.

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1. CUDA Application Analysis							
The guided analysis system walks you							
through the various analysis stages							
help you understand the optimizati opportunities in your application. C							
opportunities in your application. Once you become familiar with the optimization							
process, you can explore the individual							
analysis stages in an unguided mode.							
When optimizing your application it is important to fully utilize the compute and							
data movement capabilities of the GPU.							
To do this you should look at your							
application's overall GPU usage as well as the performance of individual kernels.							
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2 GPUs & PyTorch



The PyTorch GPU interface

The model is transferred to GPU memory with .to(device) Device can be "cpu", "cuda:0", "cuda:1" etc.

```
1 model = LeNet()
2 model = model.to("cuda:0")
```

We also send the data to GPU memory. We get data back to the CPU with the .cpu() method:

```
# Cycle through batches
1
 for idx, (data,labels) in enumerate(train_loader):
2
    data = data.to("cuda:0")
3
    optimizer.zero_grad()
4
    y = model(data)
5
    loss = crossentropy(y, labels)
6
    loss.backward()
7
    running_loss += loss.cpu().item()
8
    optimizer.step()
9
10
    _, predicted = torch.max(y.data.cpu(), 1)
11
```

PyTorch vs. Cuda

- For standard functions (Linear, Conv2d, Pooling etc.),
 PyTorch ships GPU support.
- PyTorch allows to write custom neural network layers (requiring to specify the forward and and the backward pass)
- Custom layers require CUDA programming to run on GPUs.